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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,750	11/17/2003	John A. Darringer	YOR920030418US1	3379

29683 7590 03/29/2006

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,750	DARRINGER ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17-21,52 and 53* is/are rejected.

7)☒ Claim(s) *15,16 and 22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendment + remarks filed on 3/6/06.

Claims 1-24 are and new claims 52-53 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 12-14, 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Taylor et al (US pub. 2004/0230934).

(Claim 1)

First computer program code that enables a user to specify existence of uncertainty in at least one circuit (para 0013, 0020, 0025); and

Second computer program code that automatically implements the specified uncertainty as at least one programmable circuit (para 0013, 0020, 0025).

(Claims 2, 20) further comprising third computer program code that optimizes an implementation of the at least one programmable circuit in view of at least one predetermined performance constraint (para 0034), where said at least one performance constraint comprises circuit timing imposed by clock signal constraints (para 0034).

(Claim 3) where said first computer program code implements an Uncertain Function that is used in place of a logic function or operator (para 0013, 0020).

(Claim 12) where said first computer program code implements an Uncertain Register as a register having a programmable size within a specified range (para 0006, 0011, 0020, 0022, 0029, 0032).

(Claims 13-14) where said IC is implemented at least in part as a hardwired ASIC and where said at least one programmable circuit is implemented as a FPGA (one or more of: para 0002-0008, 0012-0013, 0020, 0027, 0031, 0035, 0037); where said IC is implemented at least in part as a hardwired ASIC, and where said at least one programmable circuit is implemented as an ASIC in combination with a programmable memory component that provides at least one control input to said programmable circuit (one or more of: para 0002-0008, 0012-0013, 0020, 0027, 0031, 0035, 0037).

(Claims 17-18) where said third computer program code operates to map a circuit network obtained by operation of said first and second program code to at least one specific logic technology (one or more of: para 0002-0008, 0012-0013, 0020, 0027, 0031, 0035, 0037); where said IC is implemented at least in part as a hardwired ASIC, and where said at least one programmable circuit is implemented FPGA, and where said third computer program code operates to map FPGA components to an FPGA section of the IC and to map ASIC components to an ASIC section of the IC (one or more of: para 0002-0008, 0012-0013, 0020, 0027, 0031, 0035, 0037).

(Claim 19) where said third computer program code selects a specific technology for implementing the at least one programmable circuit (one or more of: para 0002-0008, 0012-0013, 0020, 0027, 0031, 0035, 0037) in view of the at least one performance constraint (para 0034).

(Claim 21) where optimizing comprises a consideration of required circuit area versus operational performance (fig 1)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al (US pub. 2004/0230934) in view of one or more of: Huang (USP 6618841) and Wohl (Usp 6148436).

Taylor discloses all the elements in claims except the limitations in claims 4-11.

Huang discloses the limitations in claims 4-11: where said Uncertain Function comprises an at least partly unspecified Boolean logic function with multiple inputs and multiple outputs (col 7 lines 10-41); where said Uncertain Function comprises a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions (col 7 lines 10-41); where said Uncertain Function comprises a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented (col 7 lines 10-41); wherein an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function (col 2 line 23+, col 5 lines 11-29, col 7 line 10+, also Taylor para 0034), where said Uncertain Function Assertion comprises at least one of an Input Assertion that uses a Boolean expression to specify a constraint on an input value and an Output Assertion
That uses a Boolean expression to specify a constraint on an output value (col 7 lines 10-41), where said Uncertain Function Assertion comprises an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values (col 7 lines 10-41), where said Uncertain Function Assertion comprises a Dependency Assertion for defining which inputs determine which outputs (col 2 line 23+, col 5 lines 11-29, col 7 line 10+); implementing an Uncertain Constant having a predetermined number of bits (col 10 line 31+) .

Wohl discloses the limitations in claims 4-10: where said Uncertain Function comprises an at least partly unspecified Boolean logic function with multiple inputs and multiple outputs (col 9 line 38+, col 14 line 26+); where said Uncertain Function comprises a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions (col 9 line 38+, col 14 line 26+); where said Uncertain Function comprises a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented (col 9 line 38+, col 14 line 26+); wherein an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function (col 9 line 38+, col 14 line 26+, also Taylor para 0034), where said Uncertain Function Assertion comprises at least one of an Input Assertion that uses a Boolean expression to specify a constraint on an input value and an Output Assertion

that uses a Boolean expression to specify a constraint on an output value (col 9 line 38+, col 14 line 26+), where said Uncertain Function Assertion comprises an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values (col 9 line 38+, col 14 line 26+), where said Uncertain Function Assertion comprises a Dependency Assertion for defining which inputs determine which outputs (col 9 line 38+, col 14 line 26+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use Boolean expression/logic function because Boolean expression/logic function is well known in art of logic design/test/verification and it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an Uncertain Constant having a predetermined number of bits to adhere to the non-assignable/uncertainty signal propagation logic.

New claims 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al (US pub. 2004/0230934) in view of **one or more of**: Zhang (USP 6226777), Pierce et al (USP 6256770), Yshizawa (USP 5822760), and Raynaud (USP 6240376).

Taylor discloses all the elements in claims except RTL and/or gate level description language in claims 52-53.

Zhang discloses RTL and/or gate level description language in col 1 line 15+; and

Pierce discloses RTL and/or gate level description language in col 1 line 12+; and

Yshizawa discloses RTL and/or gate level description language in col 6 line 34+; and

Raynaud discloses RTL and/or gate level description language in col 1 line 26+.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use RTL and/or gate level description language because **one or more of the followings:**

RTL and/or gate level description language are known in the art in ASIC design and synthesis (by Zhang, col 1 line 15+); and

RTL and/or gate level description language are often used in designing ASIC and systhesis process (by Pierce, col 1 line 12+); and

RTL and/or gate level description language are known to those skill in the art in systhesis and HDL (By Yshizawa, col 6 line 34+); and

RTL and/or gate level description language are process of synthesis/high level language and specified by IEEE (By Raynaud, col 1 line 26+).

Response to Applicant Remarks

The applicant states that the prior art Taylor does not disclose **computer program codes**:

*"That enables **a user to specify existence of uncertainty in at least one circuit**; and **Automatically** implements the specified uncertainty as at least one programmable circuit".*

Here is examiner answer:

Refer to fig 4; the computer program code resides within memory 412 in Computer system 400 and the computer program code is used by a designer (Para 0039) *"To enable a user to specify existence of uncertainty in at least one circuit; And automatically implements the specified uncertainty as at least one programmable circuit"*, i.e., **see one or more** the followings:

(Para 0020) "Using a software design program running on a computer platform ... a designer first chooses programmable logic blocks with known sizes and assigns these blocks to respective spaces within one or more of the FPGAs. Next, programmable logic blocks with unknown sizes or programmable logic blocks that a designer knows may change location during the design process are assigned to respective reserved spaces in each FPGA"

(Note that "computer program codes" =design software, "user" = designer; "uncertainty as at least one programmable circuit" = = programmable logic blocks with unknown sizes or programmable logic blocks that a designer knows may change location during the design process; and *"automatically"* is performed by the design software)

(Para 0023) "Blocks 105 that are representations of various logical circuits and/or programmable logic blocks as programmed by a designer during the design process. The blocks 105 may be designed using design software"

(Para 0024) "During the design process, the designer chooses the location and the

Purpose of the blocks 105 using the design software".

(Para 0025) " If the designer, however, is not sure of the best location for a particular block, as is often the case, the designer may reserve space within several FPGAs or different spaces within one FPGA and then choose later. Here, three such unknown blocks exist that need to be reserved in both FPGAs"

(Note that uncertainty as at least one programmable circuit = unsure location of programmable/FPGA blocks and/or unknown programmable/FPGA blocks)

Allowable Subject Matter

Claims 15-16, 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-16, 22-24 would be allowable because the prior art does not teach or suggest the limitations in claim 15, claim 22 and claim 24.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Primary Examiner